What is claim d is:

1. A selfaligned process for a flash memory, comprising the steps of:

depositing a first polysilicon layer, ONO layer, second polysilicon layer, a tungsten silicide and a hard mask layer in stack over a tunnel oxide layer for a gate structure having a sidewall;

forming a drain and source regions with said gate structure as a mask;

cleaning said tungsten silicide layer with a solution having a high etch selectivity to said tungsten silicide;

performing an annealing process; and

forming a spacer on said sidewall.

2. A selfaligned process according to claim 1, wherein said cleaning said tungsten silicide layer comprises applying an SC-1 solution to said tungsten silicide layer.

3. A selfaligned process according to claim 1, wherein said performing an anneal process comprises applying a rapid thermal treatment.

4. A selfaligned process for a flash memory,

comprising the steps of:

forming a gate stack including a metal silicide on a tunnel oxide layer;

forming a drain and source regions with said gate stack as a mask;

etching a sidewall of said metal silicide;

performing an annealing process; and

forming a spacer for said gate stack.

5. A selfaligned process according to claim 4, wherein said etching a sidewall of said metal silicide comprises applying a solution having a high etch selectivity to said metal silicide.

6. A selfaligned process according to claim 4, wherein said performing an anneal process comprises applying a rapid thermal treatment.

7. A selfaligned process according to claim 6, wherein said rapid thermal treatment comprises a heating in an atmosphere containing oxygen free radicals in a chamber.

8. A selfaligned process according to claim 7, wherein said rapid thermal treatment comprises providing a hydrogen and oxygen gases into said chamber.

9. A selfaligned process according to claim 8, wherein said reactor has a pressure of about 5 to 50 torrs.